4M x 4 CMOS DRAM
WITH FAST PAGE MODE, 5 VOLT

AVAILABLE AS MILITARY SPECIFICATIONS
• MIL-STD-883

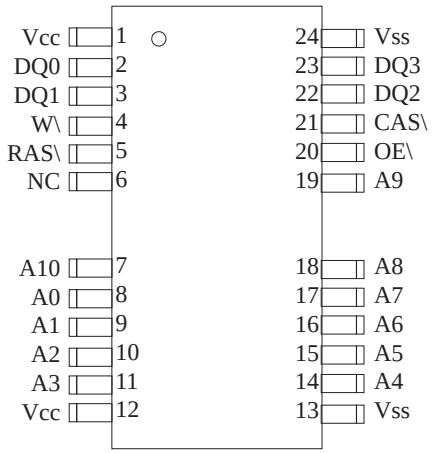
FEATURES
• Fast Page Mode Operation
• CAS\-before-RAS\ Refresh Capability
• RAS\-only and Hidden Refresh Capability
• Self-refresh Capability
• Fast Parallel Test Mode Capability
• TTL Compatible Inputs and Outputs
• Early Write or Output Enable Controlled Write
• JEDEC Standard Pinout
• Single +5V (±10%) Power Supply

OPTIONS — MARKINGS
- Timing
  - 60ns access — -6
  - 70ns access — -7
- Package
  - Plastic TSOP, 24-pin — DG
- Operating Temperature Ranges
  - Military (-55°C to +125°C) — XT
  - Industrial (-40°C to +85°C) — IT

GENERAL DESCRIPTION
The Micross Components AS4C4M4DG is a 4,194,304 x 4 bit Fast Page Mode CMOS DRAM offering high speed random access of memory cells within the same row. This device features a +5V (±10%) power supply, refresh cycle (2K), and fast access times (60 and 70ns). Other features include CAS\-before-RAS\, RAS\-only refresh, and Hidden refresh capabilities. This 4M x 4 Fast Page Mode DRAM is fabricated using an advanced CMOS process to realize high bandwidth, low power consumption and high reliability. It may be used as main memory for high level computers, microcomputers and personal computers.

For more products and information please visit our web site at
www.micross.com

PIN ASSIGNMENT
(Top View)
24 Pin TSOP (DG)



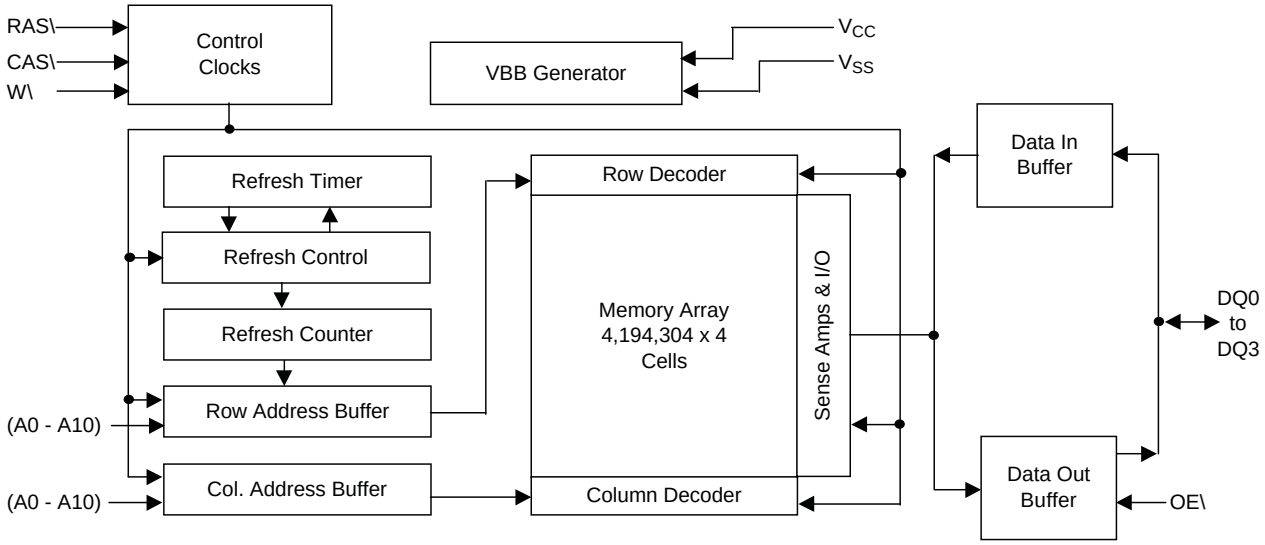
PIN ASSIGNMENT

PIN	FUNCTION
A0 - A10	Address Inputs
DQ0 -DQ3	Data In/Out
V_{SS}	Ground
RAS\	Row Address Strobe
CAS\	Column Address Strobe
W\	Read/Write Input
OE\	Data Output Enable
V_{CC}	Power (+5V)
NC	No Connect

PERFORMANCE RANGE

SPEED	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}	UNITS
-6	60	15	110	40	ns
-7	70	18	130	45	ns

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{CC} (V_{IN}, V_{OUT}).-1.0V to +7.0V
Voltage on V_{CC} supply relative to V_{SS} (V_{CC}).....-1.0V to +7.0V
Storage Temperature (T_{stg}).....-55°C to +150°C
Power Dissipation (P_D).....1W
Short Circuit Output Current (I_{OS} Address).....50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(-55°C ≤ T_A ≤ +125°C & -40°C ≤ T_A ≤ +85°C ; Vcc = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	---	V_{CC} + 0.5[1]	V
Input Low Voltage	V_{IL}	-0.5[2]	---	0.8	V

NOTES:

1. V_{CC} + 2.0V/20ns, Pulse width is measured at V_{CC}
2. -2.0V/20ns, Pulse width is measured at V_{SS}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \le T_A \le +125^oC$ & $-40^oC \le T_A \le +85^oC$; Vcc = 5V ±10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Leakage Current (any input $0 \le V_{IN} \le V_{IN}+0.5V$, all other input pins not under test = 0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	uA
Output High Voltage (I_{OH} = -5mA)	V_{OH}	2.4	---	V
Output Low Voltage (I_{OL} = 4.2mA)	V_{OL}	---	0.4	V

SYMBOL	PARAMETERS	MAX		UNITS
		-60	-70	
I_{CC1}*	Operating Current (RAS\ and CAS\, Address cycling @ t_{RC} = MIN), Power = Don't Care	110	100	mA
I_{CC2}	Standby Current (RAS\ = CAS\ = W\ = V_{IH}) Power = Normal L	3	3	mA
I_{CC3}*	RAS\-only Refresh Current (CAS\ = V_{IH}, RAS\, Address cycling @ t_{RC} = MIN), Power = Don't Care	110	100	mA
I_{CC4}*	Fast Page Mode Current (RAS\ = V_{IL}, CAS\, Address cycling @ t_{PC} = MIN), Power = Don't Care	90	80	mA
I_{CC5}	Standby Current (RAS\ = CAS\ = W\ = Vcc - 0.2V) Power = Normal L	2	2	mA
I_{CC6}*	CAS\-BEFORE-RAS\ Refresh Current (RAS\ and CAS\ cycling @ t_{RC} = MIN), Power = Don't Care	110	100	mA
I_{CC7}	Battery back-up current, Average power supply current, Battery back-up mode, Input high voltage (V_{IH}) = V_{CC} - 0.2V, Input low voltage (V_{IL}) = 0.2V, CAS\ = 0.2V, DQ = Don't care, t_{RC} = 62.5us (2K/L-ver), t_{RAS} = t_{RAS} min ~ 300ns	1	1	mA
I_{CCS}	Self Refresh Current, RAS\ = CAS\ = 0.2V, W\ = OE\ = A0 ~ A11 = V_{CC} - 0.2V or 0.2V, DQ0 ~ DQ3 = V_{CC} - 0.2V, 0.2V or Open	1	1	

NOTES:

*I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6} address can be changed maximum once while RAS\ = V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

CAPACITANCE ($T_A \leq +25^oC$; Vcc = 5V ±10%)

PARAMETER	SYMBOL	MAX	UNITS
Input capacitance (A0 - A11)	C_{IN1}	6	pF
Input capacitance (RAS\, CAS\, W\, OE\)	C_{IN2}	8	pF
Output capacitance (DQ0 - DQ3)	C_{DQ}	8	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[1,2]

($-55^oC \leq T_A \leq +125^oC$ & $-40^oC \leq T_A \leq +85^oC$; Vcc = 5V ±10%; V_{IH}/V_{IL} = 2.4/0.8V; V_{OH}/V_{OL} = 2.4/0.4V)

SYMBOL	PARAMETER	-60		-70		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	110		130		ns	
t_{RWC}	Read-modify-write cycle time	155		185		ns	
t_{RAC}	Access time from RAS\		60		70	ns	3, 4, 10
t_{CAC}	Access time from CAS\		15		20	ns	3, 4, 5
t_{AA}	Access time from column address		30		35	ns	3, 10
t_{CLZ}	CAS\ to output in Low-Z	0		0		ns	3
t_{OFF}	Output buffer turn-off delay	0	15	0	15	ns	6
t_T	Transition time (raise and fall)	3	50	3	50	ns	2
t_{RP}	RAS\ precharge time	40		50		ns	
t_{RAS}	RAS\ pulse width	60	10K	70	10K	ns	
t_{RSH}	RAS\ hold time	15		17		ns	
t_{CSH}	CAS\ hold time	60		65		ns	
t_{CAS}	CAS\ pulse width	15	10K	18	10K	ns	
t_{RCD}	RAS\ to CAS\ delay time	20	45	25	50	ns	4
t_{RAD}	RAS\ to column address delay time	15	30	17	35	ns	10
t_{CRP}	CAS\ to RAS\ precharge time	5		5		ns	
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	10		10		ns	
t_{ASC}	Column address set-up time	0		0		ns	
t_{CAH}	Column address hold time	10		12		ns	
t_{RAL}	Column address to RAS\ lead time	30		35		ns	
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time referenced to CAS\	0		0		ns	8
t_{RRH}	Read command hold time referenced to RAS\	0		0		ns	8
t_{WCH}	Write command hold time	10		12		ns	
t_{WP}	Write command pulse width	10		12		ns	
t_{RWL}	Write command to RAS\ lead time	15		17		ns	
t_{CWL}	Write command to CAS\ lead time	15		17		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[1,2] (CONTINUED)

SYMBOL	PARAMETER	-60		-70		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{DS}	Data set-up time	0		0		ns	9
t_{DH}	Data hold time	10		12		ns	9
t_{REF}	Refresh period		32		32	ms	
t_{WCS}	Write command set-up time	0		0		ns	7
t_{CWD}	CAS\ to W\ delay time	40		45		ns	7
t_{RWD}	RAS\ to W\ delay time	85		90		ns	7
t_{AWD}	Column address to W\ delay time	55		60		ns	7
t_{CPWD}	CAS\ precharge to W\ delay time	60		65		ns	
t_{CSR}	CAS\ set-up time (CAS\-before-RAS\ refresh)	5		5		ns	
t_{CHR}	CAS\ hold time (CAS\-before-RAS\ refresh)	10		15		ns	
t_{RPC}	RAS\ to CAS\ precharge time	5		5		ns	
t_{CPA}	Access time from CAS\ precharge		35		40	ns	3
t_{PC}	Fast Page cycle time	40		45		ns	
t_{PRWC}	Fast Page read-modify-write cycle time	85		95		ns	
t_{CP}	CAS\ precharge time (Fast Page Cycle)	10		10		ns	
t_{RASP}	RAS\ pulse width (Fast Page Cycle)	60	100K	70	100K	ns	
t_{RHCP}	RAS\ hold time from CAS\ precharge	35		40		ns	
t_{OEA}	OE\ access time		15		17	ns	
t_{OED}	OE\ to data delay	15		17		ns	
t_{OEZ}	Output buffer turn off delay time from OE\	0	15	0	17	ns	6
t_{OEH}	OE\ command hold time	15		17		ns	
t_{WTS}	Write command set-up time (Test mode in)	10		10		ns	11
t_{WTH}	Write command hold time (Test mode in)	10		10		ns	11
t_{WRP}	W\ to RAS\ precharge time (C\-B-R\ refresh)	10		10		ns	
t_{WRH}	W\ to RAS\ hold time (C\-B-R\ refresh)	10		10		ns	
t_{RASS}	RAS\ pulse width (C\-B-R\ self refresh)	100		110		us	13, 14, 15
t_{RPS}	RAS\ precharge time (C\-B-R\ self refresh)	110		120		ns	13, 14, 15
t_{CHS}	CAS\ hold time (C\-B-R\ self refresh)	-50		-50		ns	13, 14, 15

TEST MODE CYCLE[11]

SYMBOL	PARAMETER	-60		-70		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	115		135		ns	
t_{RWC}	Read-modify-write cycle time	160		180		ns	
t_{RAC}	Access time from RAS\		65		70	ns	3, 4, 10, 12
t_{CAC}	Access time from CAS\		20		22	ns	3, 4, 5, 12
t_{AA}	Access time from column address		35		38	ns	3, 10 ,12
t_{RAS}	RAS\ pulse width	65	10K	75	10K	ns	
t_{CAS}	CAS\ pulse width	20	10K	25	10K	ns	
t_{RSH}	RAS\ hold time	20		22		ns	
t_{CSH}	CAS\ hold time	65		70		ns	
t_{RAL}	Column address to RAS\ lead time	35		40		ns	
t_{CWD}	CAS\ to W\ delay time	45		48		ns	7
t_{RWD}	RAS\ to W\ delay time	90		100		ns	7
t_{AWD}	Column address to W\ delay time	60		70		ns	7
t_{CPWD}	CAS\ precharge to W\ delay time	65		70		ns	
t_{PC}	Fast Page cycle time	45		50		ns	
t_{PRWC}	Fast Page read-modify-write time	90		100		ns	
t_{RASP}	RAS\ pulse width (Fast Page Cycle)	65	100K	75	100K	ns	
t_{CPA}	Access time from CAS\ precharge		40		45	ns	3
t_{OEA}	OE\ access time		20		22	ns	
t_{OED}	OE\ to data delay	20		22		ns	
t_{OEH}	OE\ command hold time	20		22		ns	

NOTES:

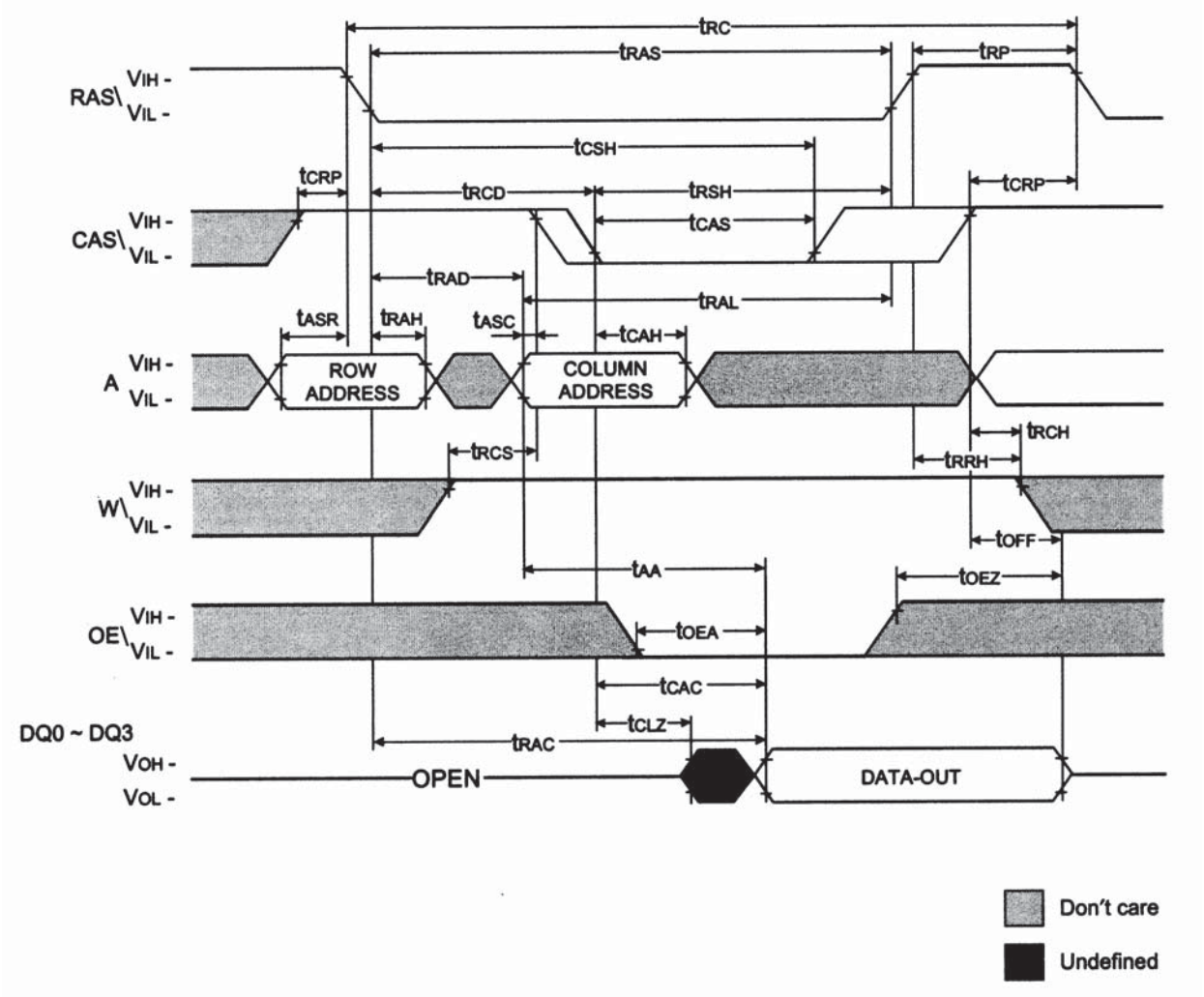
1. An initial pause of 200us is required after power-up followed by an 8 RAS\-only refresh or CAS\-before-RAS\ refresh cycles before proper device operation is achieved.
2. V_{IH}(MIN) and V_{IL}(MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(MIN) and V_{IL}(MAX) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(MAX) limit insures that t_{RAC}(MAX) and be met. t_{RCD}(MAX) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(MAX) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(MAX).
6. t_{OFF}(MIN) and t_{OEZ}(MAX) define the time at which the output achieves the open circuit condition and are not referenced V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(MIN), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(MIN), $t_{RWD} \geq t_{RWD}$(MIN) and $t_{AWD} \geq t_{AWD}$(MIN), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

(Continued on page 7)

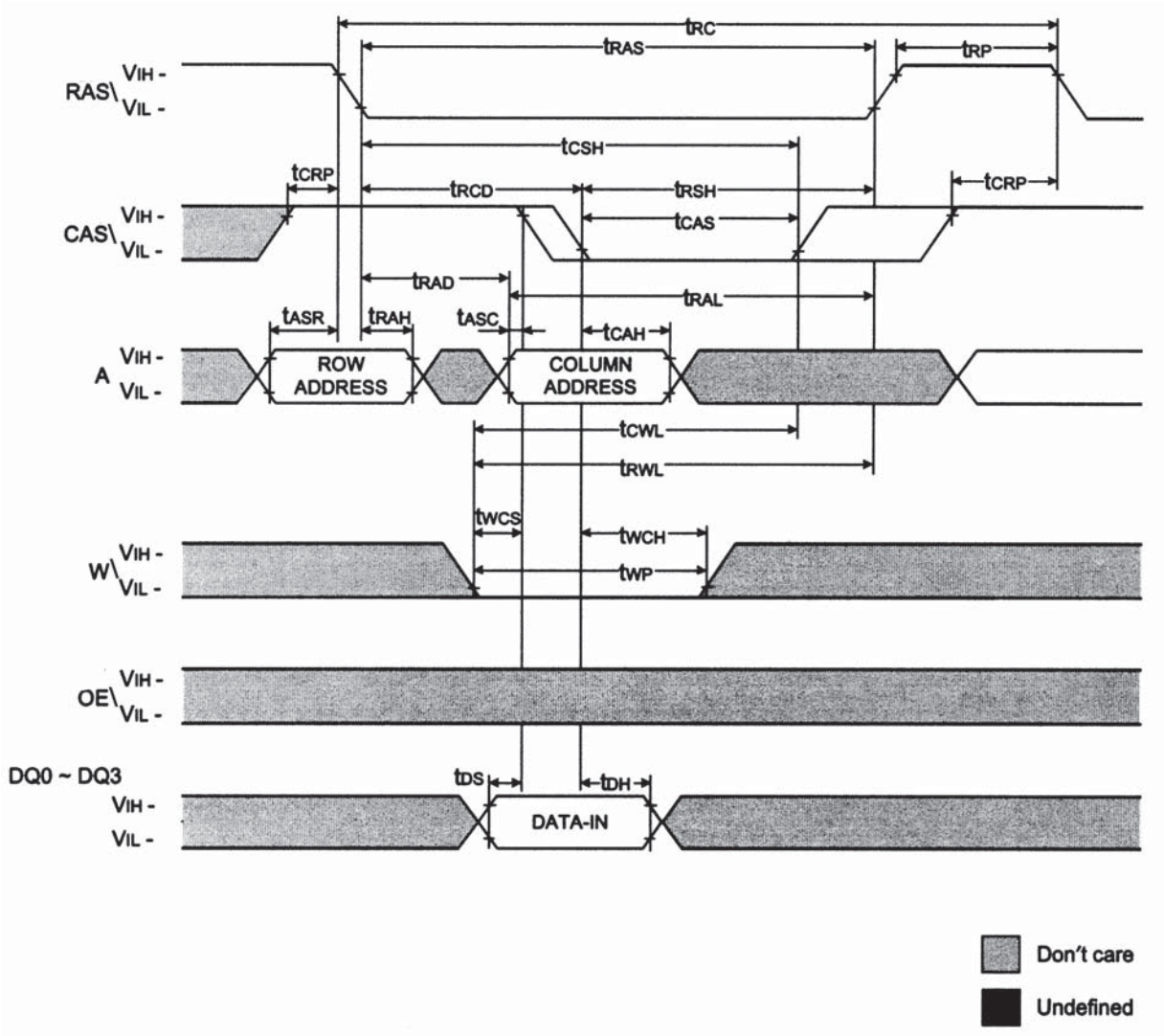
NOTES (continued):

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to CAS\ falling edge in early write cycles and to W\ falling edge in read-modify-write cycles.
10. Operation within the t_{RAD}(MAX) limit insures that t_{RAC}(MAX) can be met. t_{RAD}(MAX) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAS}(MAX) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If $t_{RASS} \geq 100$ us, then RAS\ precharge time must use t_{RPS} instead of t_{RP}.
14. For RAS\-only refresh and burst CAS\-before-RAS\ refresh mode, 2048 cycles of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.
15. For distributed CAS\-before-RAS\ with 15.6us interval CAS\-before-RAS\ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

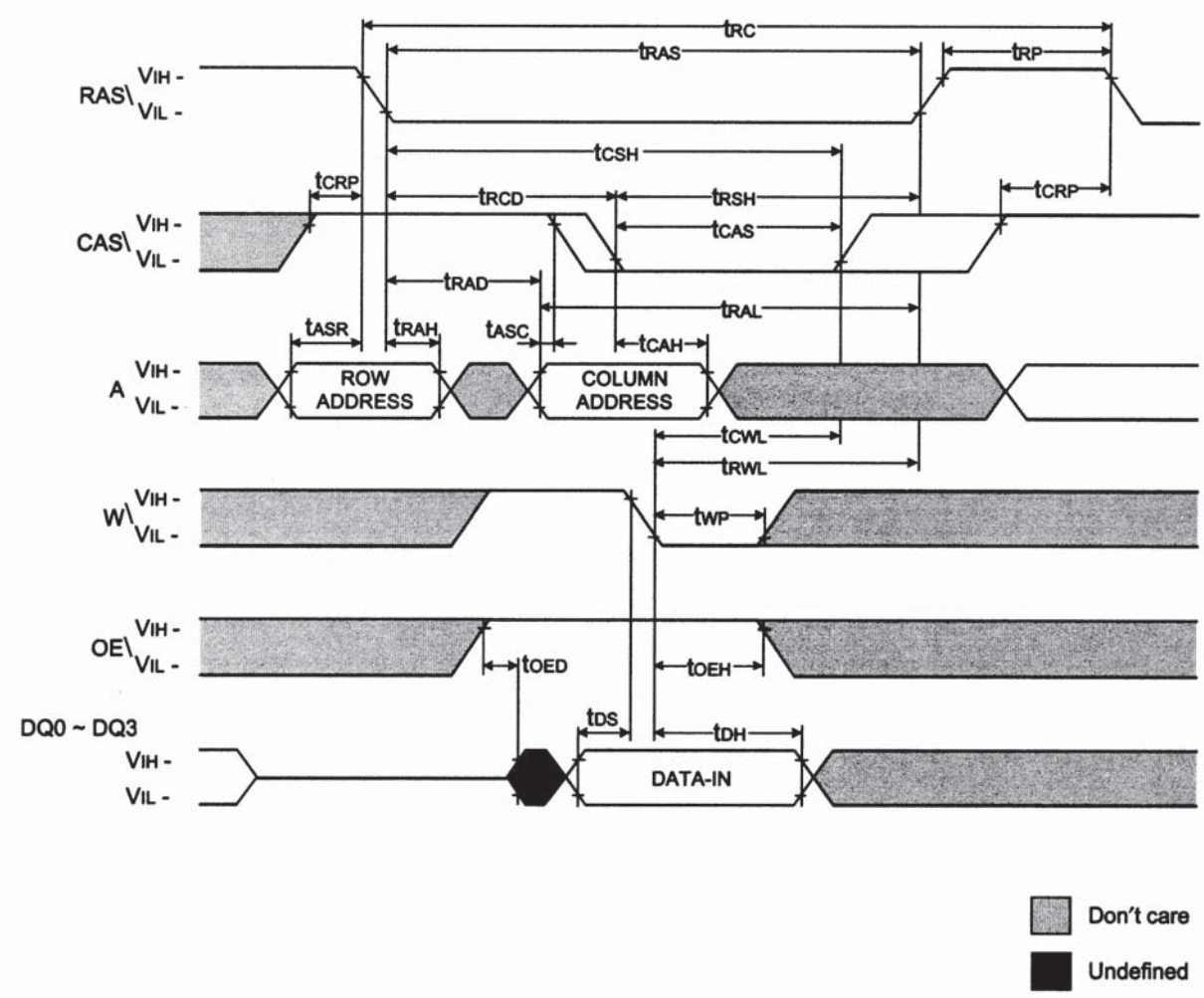
READ CYCLE



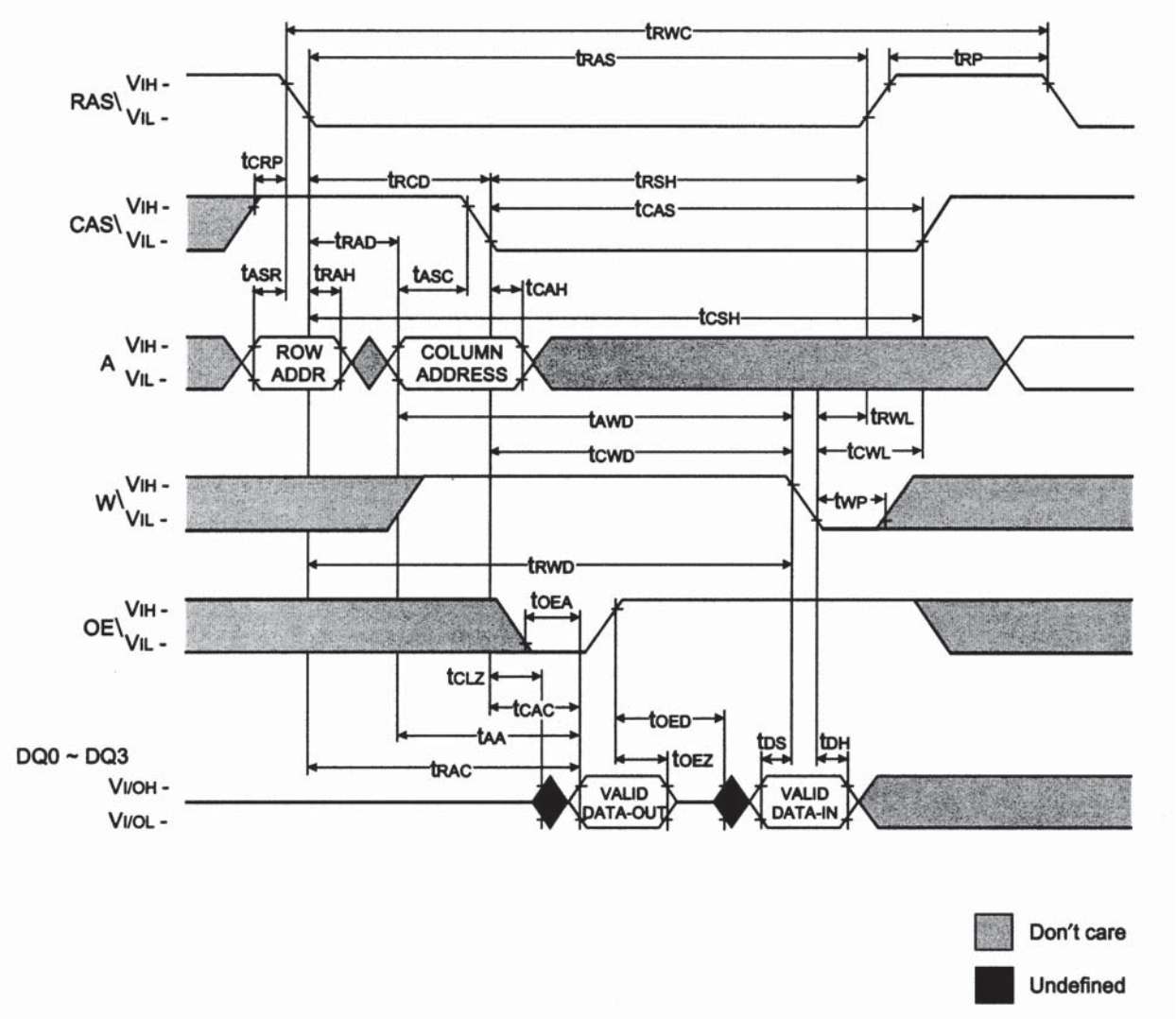
WRITE CYCLE (EARLY WRITE) D_{OUT} = OPEN



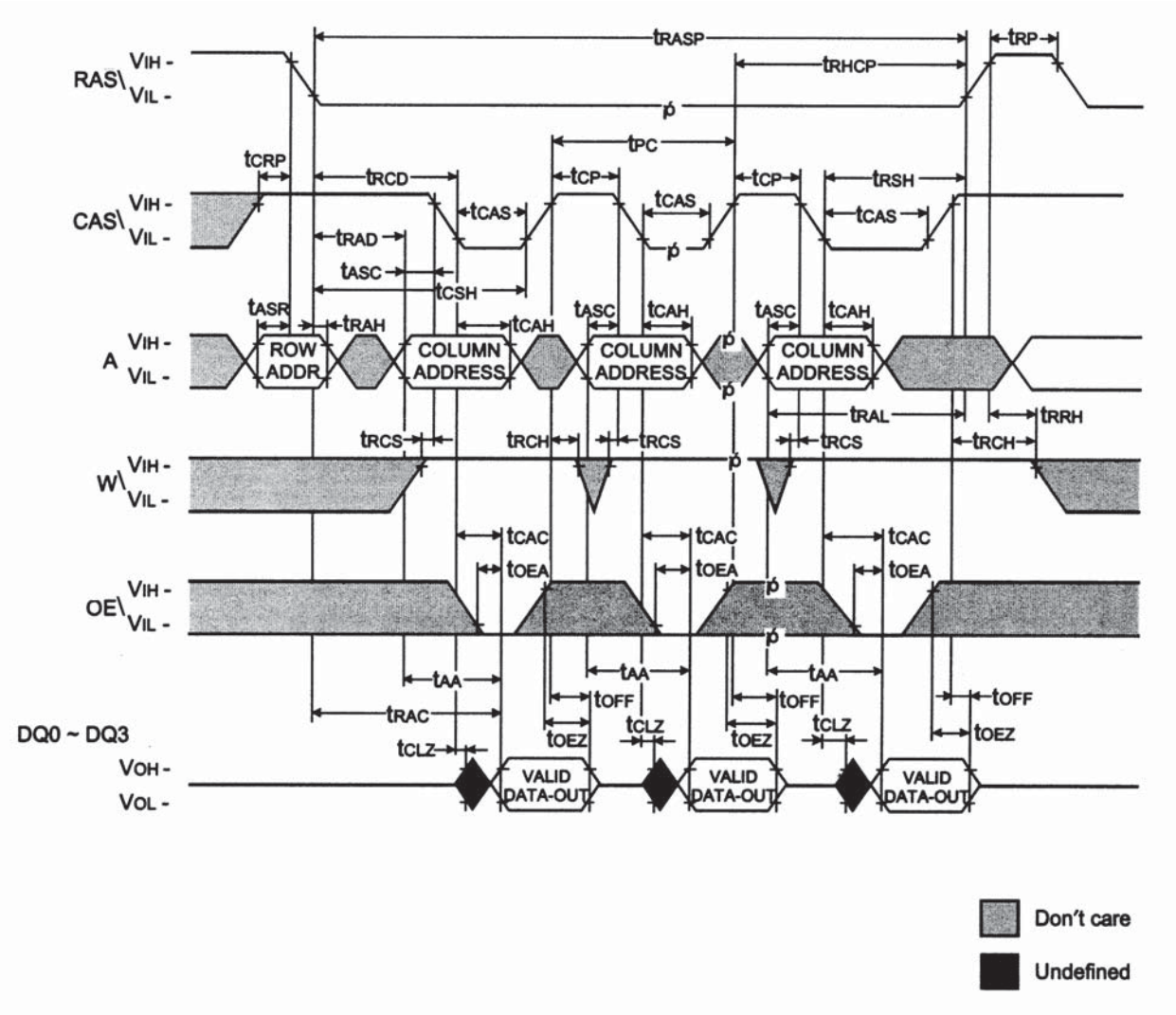
WRITE CYCLE (OE\ CONTROLLED WRITE) D_{OUT} = OPEN



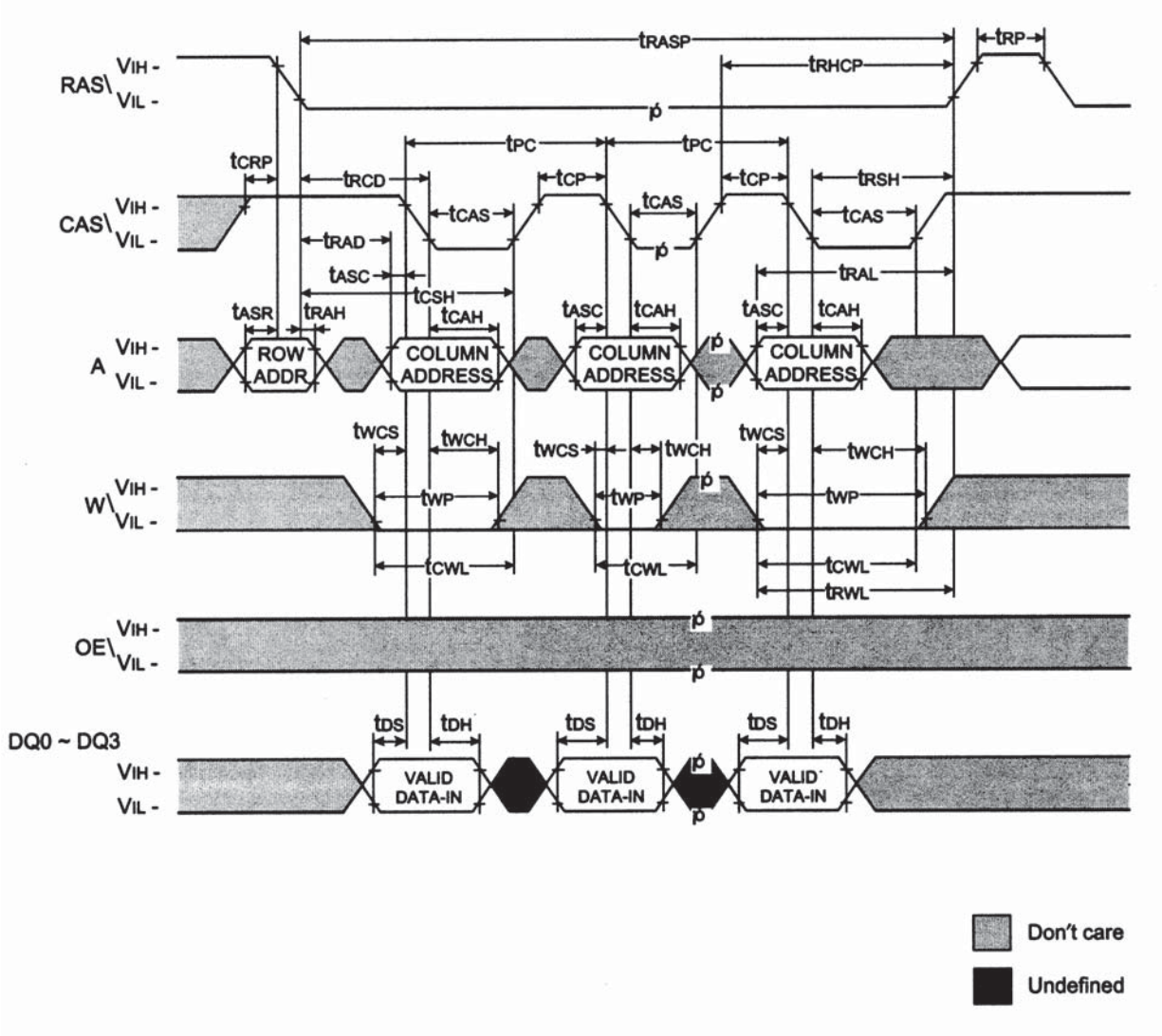
READ-MODIFY-WRITE CYCLE



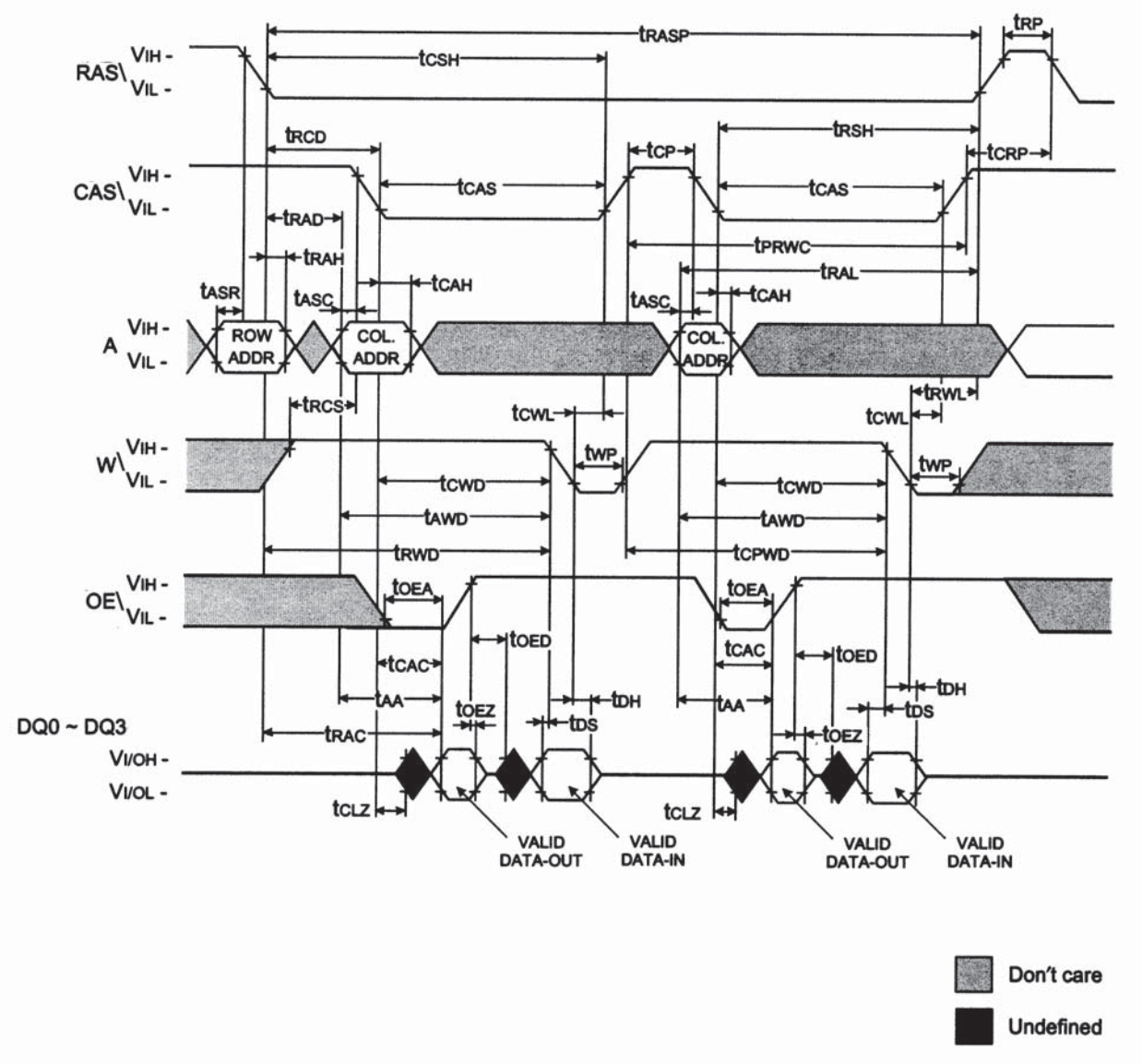
FAST PAGE READ CYCLE



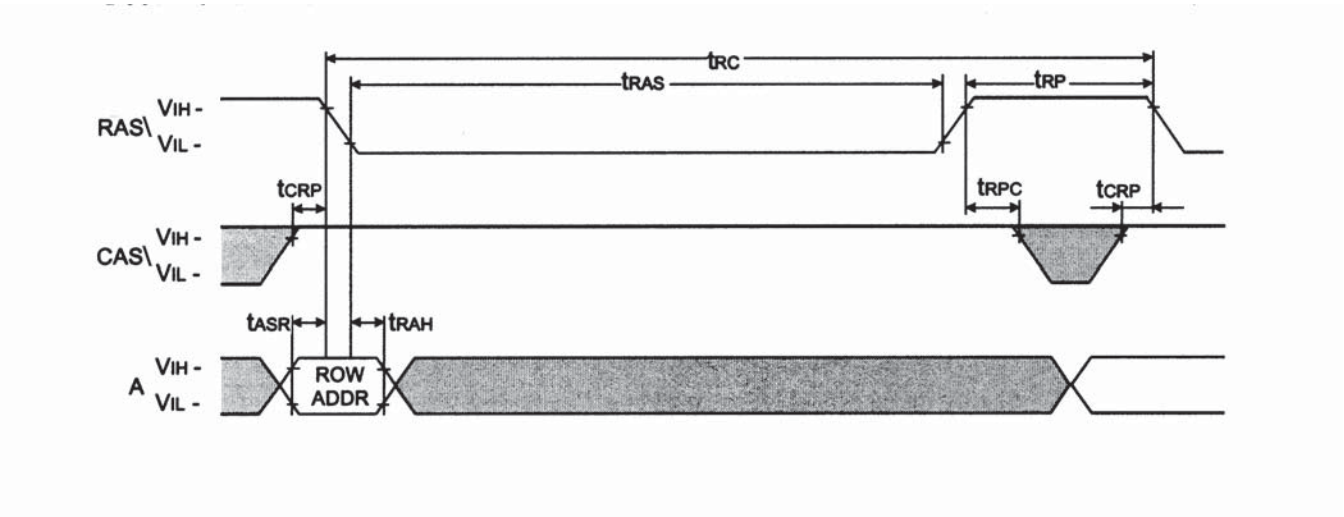
FAST PAGE WRITE CYCLE (EARLY WRITE) D_{OUT} = OPEN



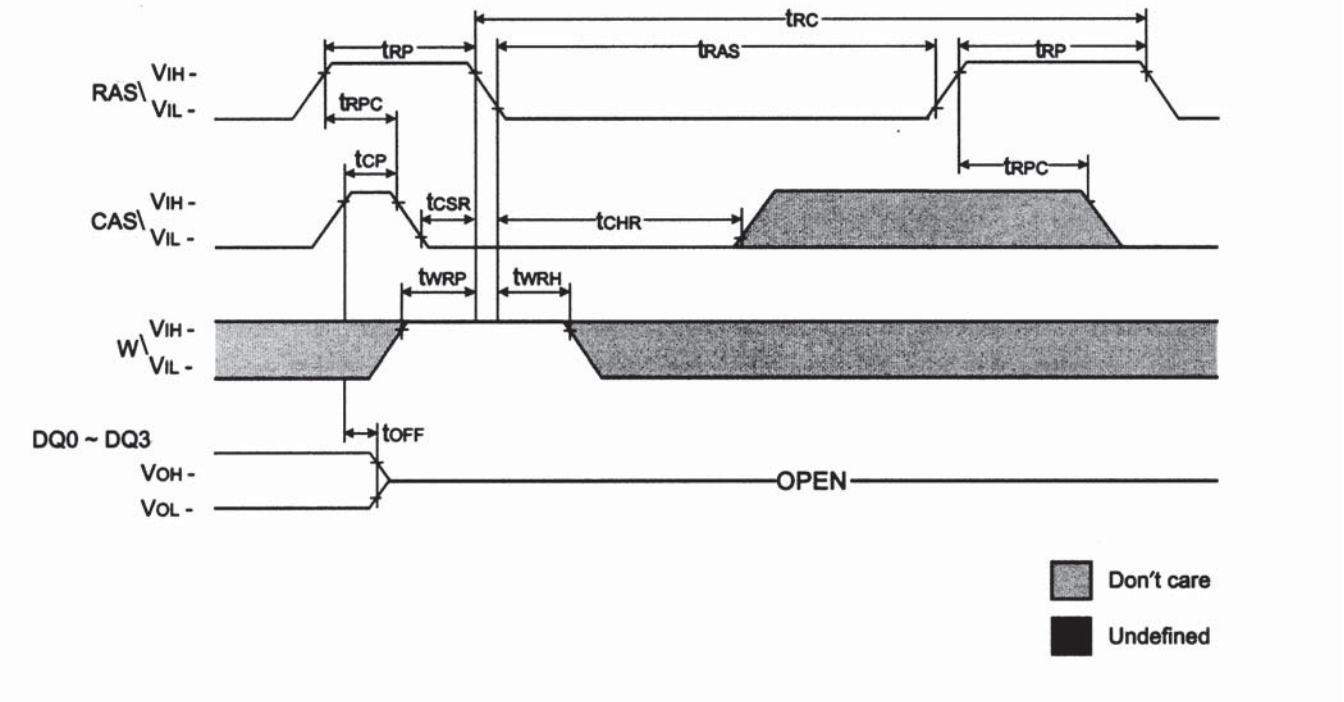
FAST PAGE READ-MODIFY-WRITE CYCLE



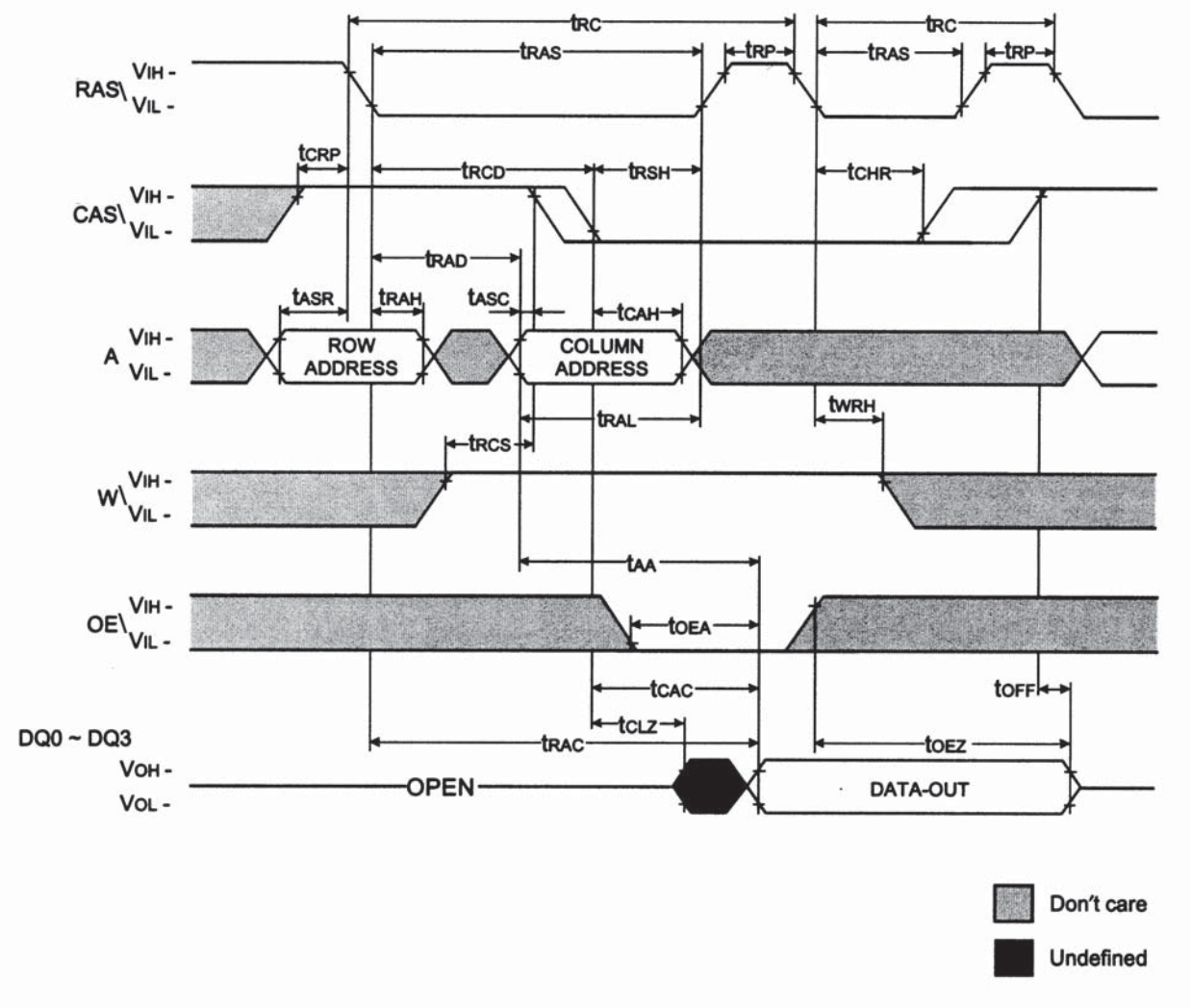
RAS\-ONLY REFRESH CYCLE (W\, OE\, D_{IN} = DON'T CARE; D_{OUT} = OPEN)



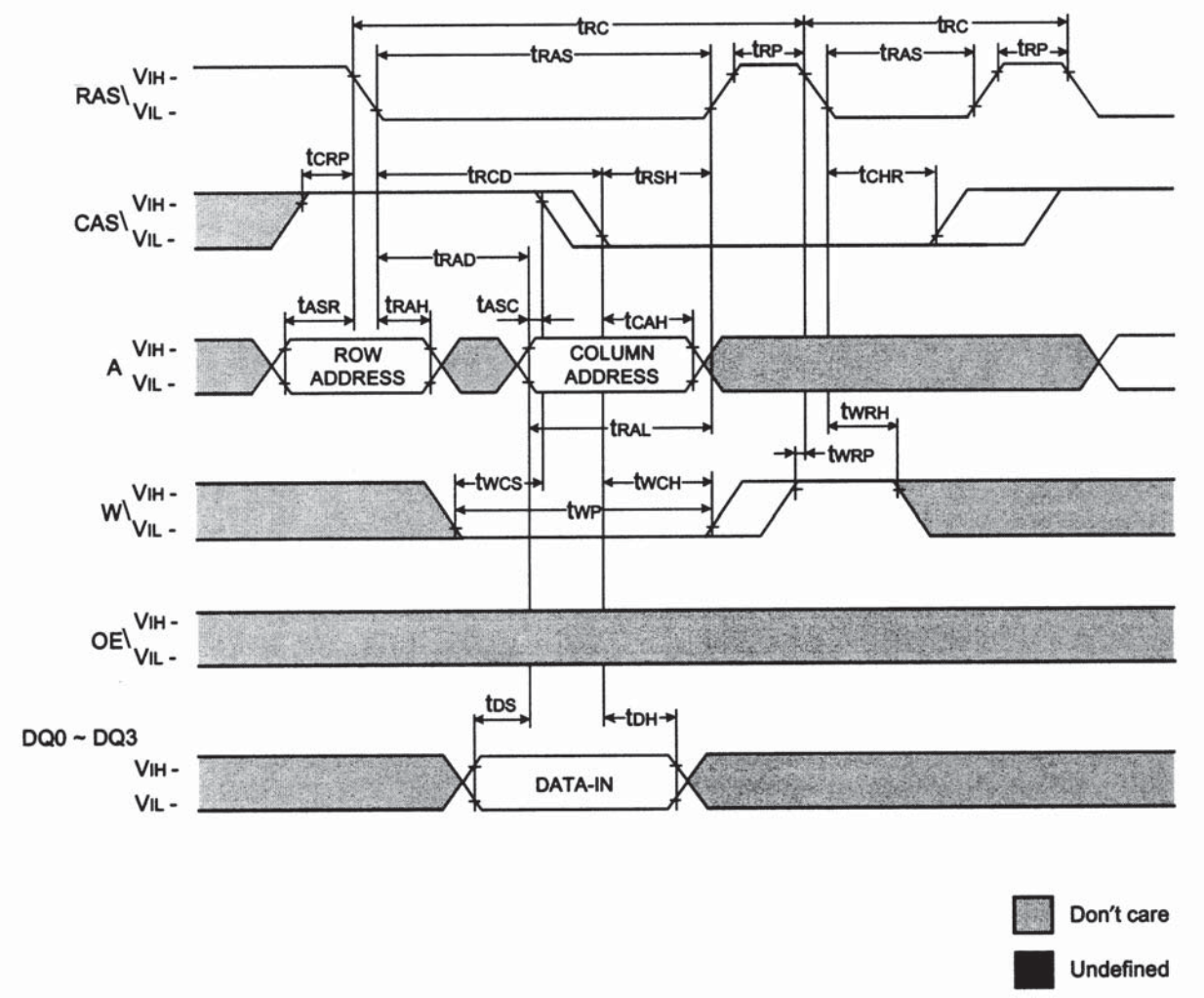
CAS\-BEFORE-RAS\ REFRESH CYCLE (OE\, A = DON'T CARE)



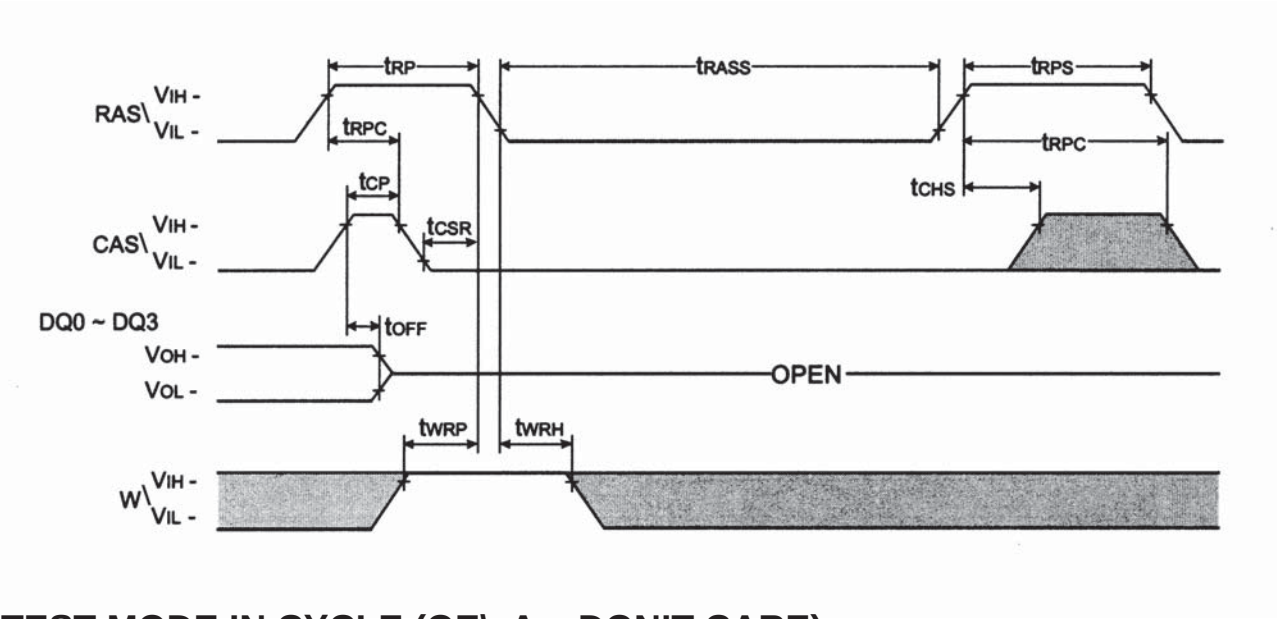
HIDDEN REFRESH CYCLE (READ)



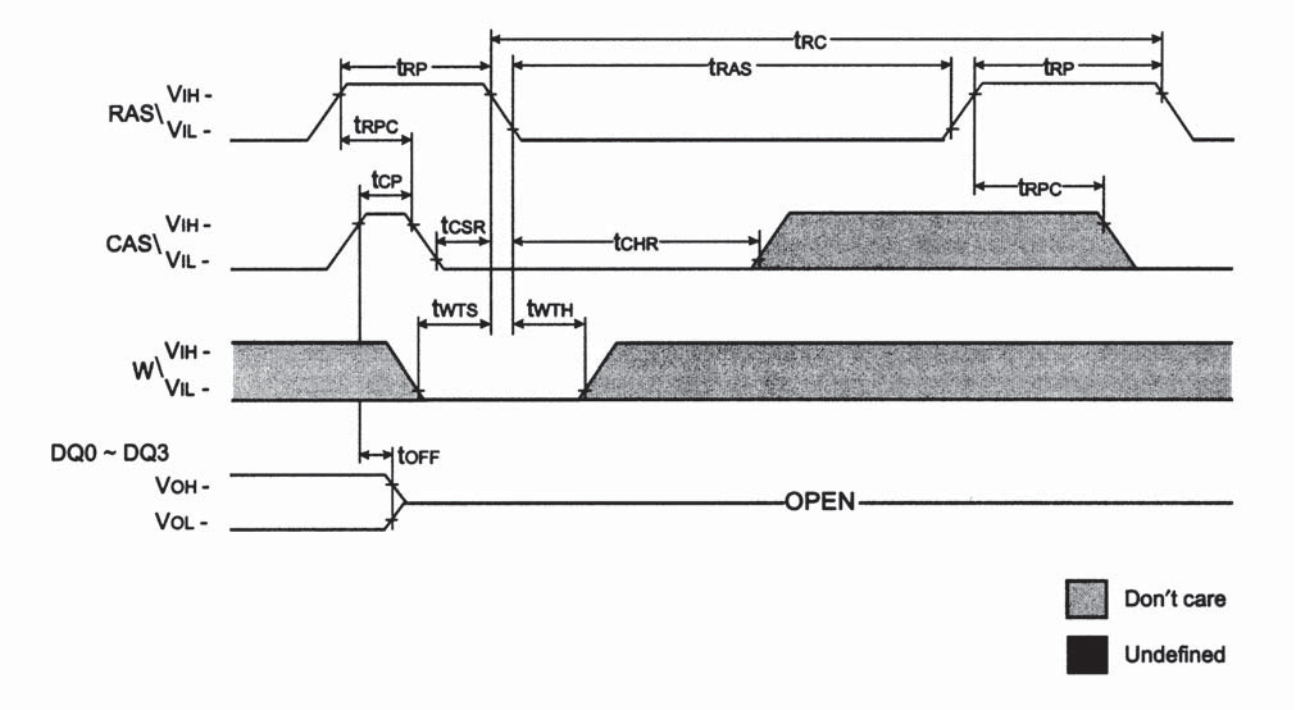
HIDDEN REFRESH CYCLE (WRITE) D_{OUT} = OPEN



CAS\-BEFORE-RAS\ SELF REFRESH CYCLE (OE\, A = DON'T CARE)

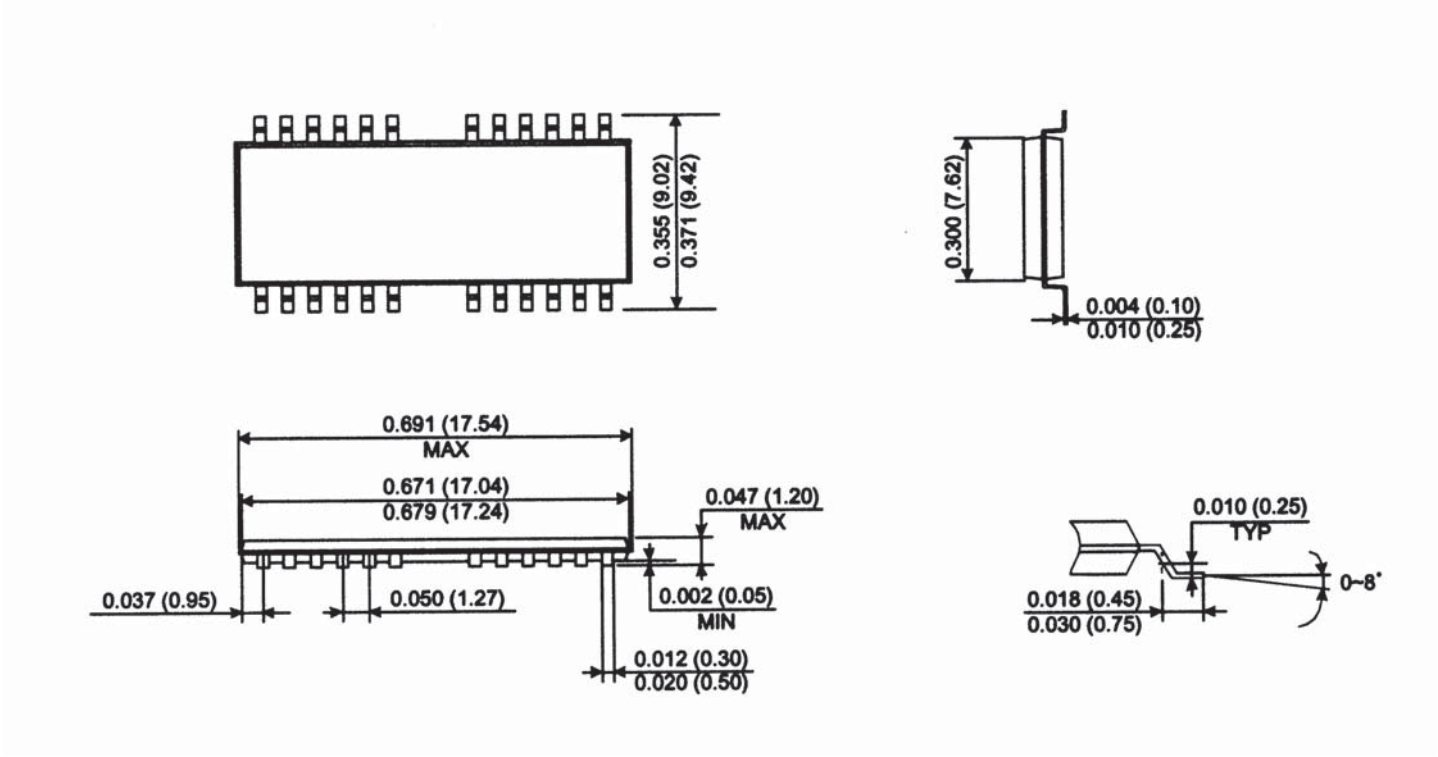


TEST MODE IN CYCLE (OE\, A = DON'T CARE)



MECHANICAL DEFINITIONS*

Package Designator DG



**All measurements are in inches (millimeters).*

ORDERING INFORMATION

EXAMPLE: AS4C4M4DG-7/IT

Device Number	Package Type	Speed	Process
AS4C4M4	DG	-6	/*
AS4C4M4	DG	-7	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Military Temperature Range -55°C to +125°C